the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Claims 1, 8, 14, 21, 27 and 33 recite that noise due to the first and the second signals is reduced by the phase difference. For the reasons provided below, Misawa, Nakano and Prak, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action asserts that Figure 11 of Misawa discloses the following (page 2, Paper No. 20061031; emphasis added):

> ... a pair of dual clocks signal for driving a shift register having a first clock signal CL (first signal) and a reversed clock signal CL (second signal) having a different phase from the first clock signal (first signal), and both the clock signal and the reversed clock signal (first signal and second signal) are transmitted to each of shift register unit cells. Misawa teaches

noise [due] to the first and the second signals is reduced by the phase difference (col. 12, lines 31-34).

The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The Official Action appears to argue that the phase difference in Misawa is caused by inverting a fist clock signal CL (a first signal). In the "Response to Arguments" section, the Official Action refers to Figures 11A and Figure 11B, and column 12, lines 31-34, to support the assertion that noise due to first and second signals is reduced by phase difference (page 6, Paper No. 20061031). The Applicant disagrees.

Misawa clearly teaches that "source line driver circuit 12 is provided with ... a line for transmitting at least a pair of dual clock signals CL and $\overline{CL}$ for driving shift register 13. If there is a difference between stray capacitance formed between video signal bus 36 and the CL line and the stray capacitance formed between video signal bus 36 and the $\overline{CL}$ line, noise in the form of spike synchronizing with the clock signal is unintentionally added to the video signal" (see column 12, lines 2-12). That is, Misawa appears to disclose that noise occurs by inputting the dual clock signals CL and $\overline{CL}$ for a driving shift register. This is not the same as reducing noise by a phase difference. This disclosure of Misawa appears to correspond to Figure 5 of the present specification, which is part of the description of related art.

Specifically, in order to reduce noise, Misawa discloses that the rising edge of CL corresponds to the trailing edge of $\overline{CL}$ and the rising edge of $\overline{CL}$ corresponds to the trailing edge of CL (see column 12, lines 29-32). The plain language of Misawa is contrary to the assertion in the Official Action. This feature is also disclosed in the description of related art in the present specification at page 4, lines 6-16. Therefore, the Applicant respectfully submits that Misawa does not teach or suggest that noise due to the first and the second signals is reduced by the phase difference.

Further, the Official Action asserts that "in order to make and use Misawa's device with two different phase clock signals, it would have been obvious ... to modify the control circuit of Misawa as modified by Nakano to have a delay circuit as taught by Prak" (page 3, Paper No. 20061031). As noted above, Misawa does not appear to teach or suggest that phase difference reduces noise. Prak does not cure the deficiencies in Misawa. Although Prak teaches that the delay means 12 outputs a delay signal BPH1D, which "prevents the phase two clocking signal from overlapping the phase one clocking signal" (column 2, lines 32-53), Prak does not explain why one of ordinary skill in the art at the time of the present invention would have modified Misawa such that noise due to the first and the second signals is reduced by phase difference instead of by making the rising edge of CL correspond to the trailing edge of $\overline{CL}$ and by making the rising edge of $\overline{CL}$ correspond to the trailing edge of CL. In other words, the alleged motivation for combining Misawa and Prak ("a minimum of skew") can be achieved from the device of Prak alone and thus there is no need to combine the device of Prak with Misawa. Rather, since Misawa fails to recognize this as a problem, one of skill in the art would merely be led to practice Prak alone in view of the asserted motivation.

Nakano does not cure the deficiencies in Misawa and Prak. Nakano is relied upon to allegedly teach a control circuit for generating a clock signal and a video signal processing circuit (Id.). However, Nakano does not teach or suggest that noise due to the first and the second signals is reduced by the phase difference. Also, Nakano does not teach or suggest that a first signal and second signal which has a different phase from the first signal are input to a shift register. Therefore, it is not clear why one would have been motivated to apply the teachings of Nakano to Misawa and Prak.

Furthermore, Prak does not teach or suggest the features of dependent claims 39-44, which recite that a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time of the first signal, and shorter than a half of a signal holding timer period. The Official Action asserts that Figure 5 of Prak shows

this feature (page 5, Id.). The Applicant respectfully disagrees and traverses the assertion in the Official Action. Figure 5 of Prak appears to show "a delay, represented by line 60, introduced by the feedback loop, between the falling edge of the phase two signal and the rising edge of the phase one signal so that the phase one signal and the phase two signal do not overlap" (column 2, lines 49-53). Prak does not teach or suggest that a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time of the first signal, and shorter than a half of a signal holding timer period.

Since Misawa, Nakano and Prak do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 4 of the Official Action rejects claims 7, 13, 20, 26, 32 and 38 as obvious based on the combination of Misawa, Nakano, Prak and U.S. Patent No. 5,801,678 to Shimada.

Please incorporate the arguments above with respect to the deficiencies in Misawa, Nakano and Prak. Shimada does not cure the deficiencies in Misawa, Nakano and Prak. The Official Action relies on Shimada to allegedly teach the features of the dependent claims (page 6, Id.). Specifically, the Official Action relies on Shimada to allegedly teach a projection type display device. However, Misawa, Nakano, Prak and Shimada, either alone or in combination, do not teach or suggest that noise due to the first and the second signals is reduced by the phase difference. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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